ADM-PCIE-9H7
User Manual

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1 Introduction

The ADM-PCIE-9H7 is a high-performance reconfigurable computing card intended for Data Center applications, featuring a Xilinx Virtex UltraScale+ Plus FPGA with High Bandwidth Memory (HBM).

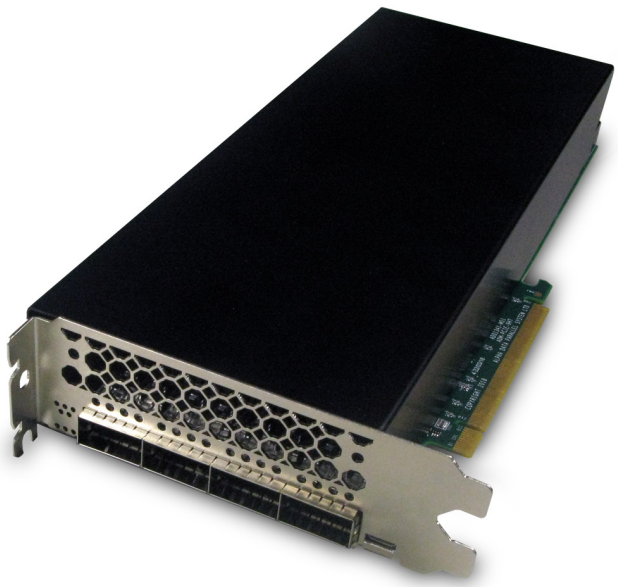

Figure 1 : ADM-PCIE-9H7 Product Photo

1.1 Key Features

Key Features

- PCIe Gen1/2/3 x1/2/4/8/16 capable
- Passive and active thermal management configuration
- 3/4 length, full height, 2 slot, x16 edge PCIe form factor (GPU size)
- 8GB HBM on-die memory capable of 460GB/s
- Four QSFP28 cages capable of data rates up to 28 Gbps per channel (112 Gbps per cage)
- Two 8 lane Ultraport SlimSAS connectors compliant with OpenCAPI
- Supports either VU35P or VU37P Virtex UltraScale+ FPGAs
- Eight (VU37P) or four (VU35P) FireFly sites capable of data rates up to 28 Gbps per channel (112 Gbps per site)
- Front panel and rear edge JTAG access via USB port
- FPGA configurable over USB/JTAG and SPI configuration flash
- Voltage, current, and temperature monitoring
- 16 GPIO signals and 1 isolated timing input

1.2 Order Code

ADM-PCIE-9H7

See the datasheet for complete ordering options.

2 Board Information

2.1 Physical Specifications

The ADM-PCIE-9H7 complies with PCI Express CEM revision 3.0.

Description	Measure
PCB Dy	111.15 mm
PCB Dx	254 mm
PCB Dz	1.6 mm

Table 1 : Mechanical Dimensions (PCB only)

Description	Measure
Total Dy	125.2 mm
Total Dx	267.2 mm
Total Dz	41.9 mm
Weight	1300 grams

Table 2 : Mechanical Dimensions (Fully Assembled)

2.2 Chassis Requirements

2.2.1 PCI Express

The ADM-PCIE-9H7 is capable of PCIe Gen 1/2/3 with 1/2/4/8/16 lanes, using the Xilinx Integrated Block for PCI Express.

2.2.2 Mechanical Requirements

A 16-lane physical PCIe slot is required for mechanical compatibility.

2.2.3 Power Requirements

The ADM-PCIE-9H7 has a PCIe Auxiliary power connector on the back edge. This must be used in combination with the PCIe edge connector order for the board to power up. The total power envelope for the card is 225W.

The power sense signals as defined in the PCIe CEM are available to the FPGA for integration into user logic. It is highly recommended that if the application requires more than 150W available between the 6-pin Auxiliary plug and PCIe edge, the sense pins are interrogated to ensure the 8-pin 150W connector is present. For constraint information, see net names PWR_SENSE0_PIN, and PWR_SENSE1_PIN in Complete Pinout Table.

The PCIe Specification permits a standard full-height, double slot PCIe card to dissipate up to 225 W of power, drawn from the PCIe slot and auxiliary connector combined. Power consumption estimation requires the use of the Xilinx XPE spreadsheet and a power estimator tool available from Alpha Data. Please contact **support@alpha-data.com** to obtain this tool.

The power available to the rails calculated using XPE are as follows:

Voltage	Source Name	Current Capability
0.72-0.90	VCC_INT	102A
0.85-0.90	VCCINT_IO + VCC_BRAM	25A
0.9	MGTAVCC	14A
1.2	MGTAVTT	25A
1.2	VCC_HBM * VCC_IO_HBM	18A
1.8	VCCAUX + VCCAUX_IO + VCCO_1.8V	7A
1.8	MGTVCCAUX	1A
2.5	VCCAUX_HBM	2A
3.3	3.3V for Optics	25A

Table 3 : Available Power By Rail

2.3 Thermal Performance

If the FPGA core temperature exceeds 105 degrees Celsius, the FPGA design will be cleared to prevent the card from over-heating.

The ADM-PCIE-9H7 comes with a heat sink to reduce the heat of the FPGA which is typically the hottest point on the card. The FPGA die temperature must remain under 100 degrees Celsius. To calculate the FPGA die temperature, take your application power and multiply by Theta JA from the table below, and add to your system internal ambient temperature. If you are using the fan provided with the board, you will find theta JA is approximately 0.4 degC/W for the board in still air.

The power dissipation can be estimated by using the Alpha Data power estimator in conjunction with the Xilinx Power Estimator (XPE) downloadable at http://www.xilinx.com/products/technology/power/xpe.html . Download the UltraScale tool and set the Device to Virtex UltraScale+, VU37P or VU35P, FSVH2892, -2 or -3, Extended. Set the ambient temperature to your system ambient and select User Override for the Effective theta JA and enter the figure associated with your system LFM in the blank field. Proceed to enter all applicable design elements and utilization in the following spreadsheet tabs. Next aquire the 9H7 power estimator from Alpha Data by contacting support@alpha-data.com. You will then plug in the FPGA power figures along with Optical module figures to get a board level estimate.

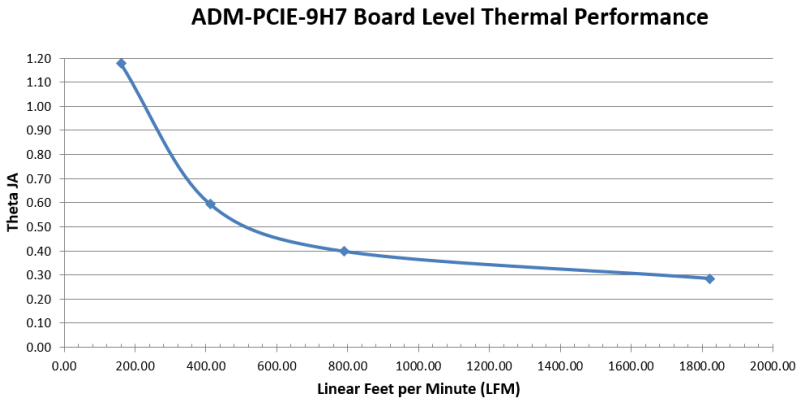

Figure 2 : Thermal Performance

2.3.1 Active VS Passive Thermal Management

Because it is likely a generic PC chassis to not provide sufficient airflow to cool the card, the ADM-PCIE-9H7 default built utilizes the active cooling configuration with fans installed to force air across the heat sink. If the ADM-PCIE-9H7 will be installed in a server with good controlled airflow, the order option /NF can be used to receive cards in the passive cooling configuration with the fans removed. The fans have a much shorter mean time between failure (MTBF) than the rest of the assembly, so passive cards have much longer life expectance before requiring maintenance. The ADM-PCIE-9H7 also includes fan speed controllers, allowing variable fan speed based on die temperature, and detection of failed fans (see section Fan Controllers).

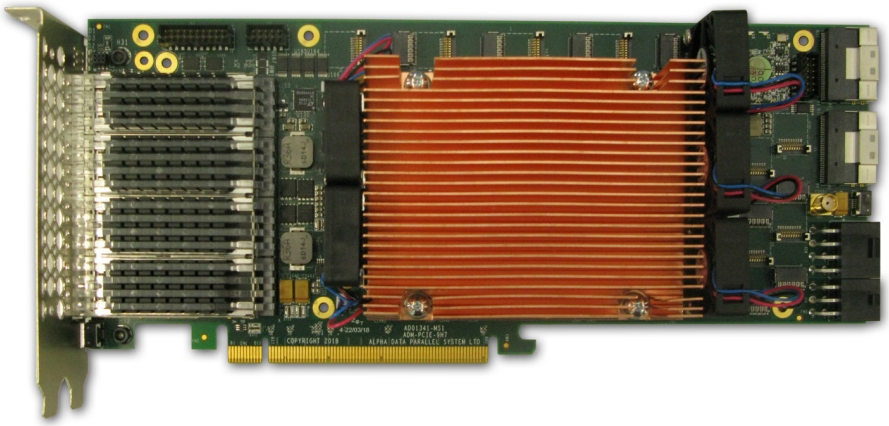

Figure 3 : ADM-PCIE-9H7 Heat Sink with Fans

3 Functional Description

3.1 Overview

The ADM-PCIE-9H7 is a versatile reconfigurable computing platform with a Virtex UltraScale+ VU37P or VU35P FPGA, a Gen3x16 PCIe interface, 8GB of HBM memory, four QSFP28 cages plus 8 FireFly sites (4 FireFly with a VU35P) each capable of 4x 28G or 1x 112G Serial IO of any Xilinx supported standard (Ethernet, SRIO, Infiniband, etc.), two OpenCAPI compatible Ultraport SlimSAS connector also capable of 28G/channel, an isolated input for a timing synchronization pulse, a 20 pin header for general purpose use (clocking, control pins, debug, etc.), and a robust system monitor.

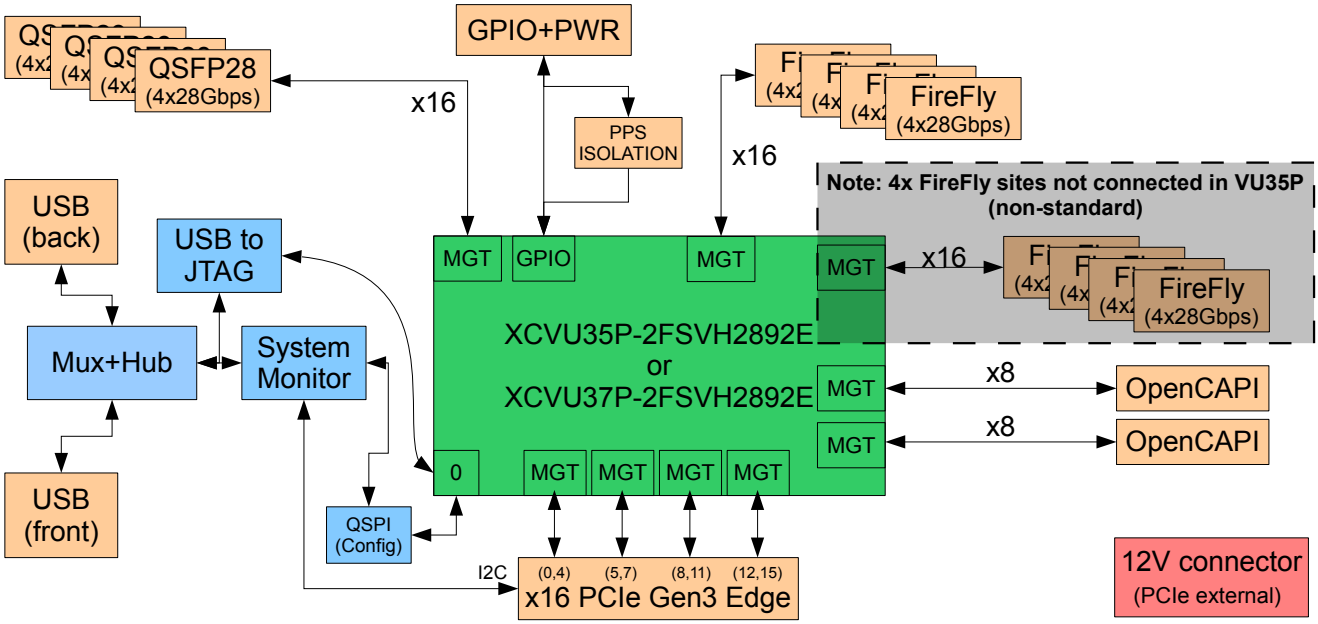

Figure 4 : ADM-PCIE-9H7 Block Diagram

3.1.1 Switches

The ADM-PCIE-9H7 has an octal DIP switch SW1, located on the rear side of the board. The function of each switch in SW1 is detailed below:

Figure 5 : Switches

Switch	Factory Default	Function	OFF State	ON State
SW1-1	OFF	User Switch 0	Pin BF52 = '1'	Pin BF52 = '0'
SW1-2	OFF	User Switch 1	Pin BF47 = '1'	Pin BF47 = '0'
SW1-3	OFF	Reserved	Reserved	Reserved
SW1-4	OFF	Power Off	Board will power up	Immediately power down
SW1-5	OFF	Service Mode	Regular Operation	Firmware update service mode
SW1-6	ON	HOST_I2-C_EN	Sysmon over PCIe I2C	Sysmon isolated
SW1-7	ON	CAPI_VP-D_EN	OpenCAPI VPD available	OpenCAPI VPD isolated
SW1-8	ON	CAPI_VP-D_WP	CAPI VPD is write protected	CAPI VPD is writable

Table 4 : Switch Functions

Use IO Standard "LVCMOS18" when constraining the user switch pins.

3.1.2 LEDs

There are 24 LEDs on the ADM-PCIE-9H7, 21 of which are general purpose and whose meaning can be defined by the user. The other 3 have fixed functions described below:

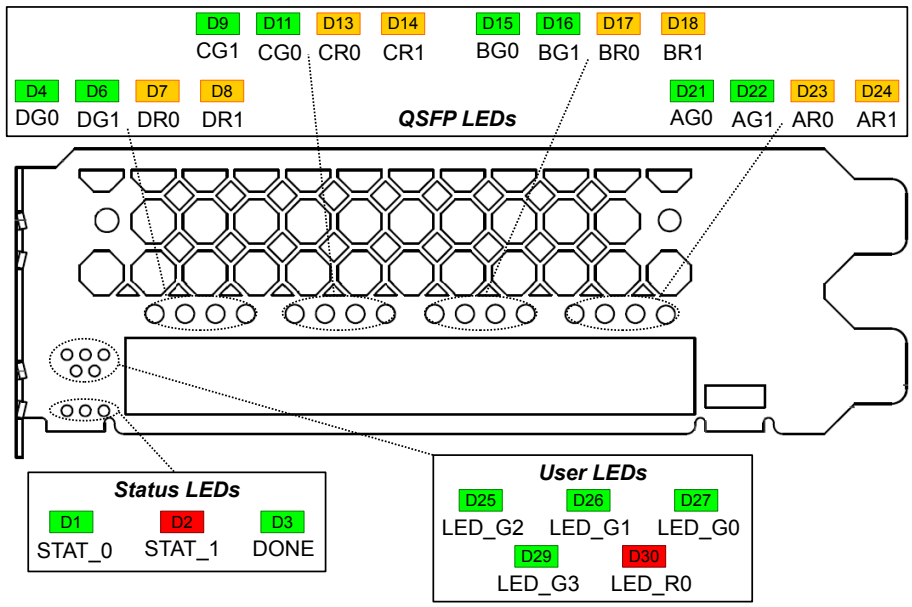

Figure 6 : Front Panel LEDs

Comp. Ref.	Function	ON State	OFF State
D1	Status 0	See Status LED Definitions	
D2	Status 1	See Status LED Definitions	
D3	DONE	FPGA is configured	FPGA is not configured
D4-D24	QSFP_LED_*	User defined '0'	User defined '1'
D25-D30	USER_LED_*	User defined '0'	User defined '1'

Table 5 : LED Details

See Section Complete Pinout Table for full list of user controlled LED nets and pins

Rev 1 PCBs LED nets QSFP_LED_CG0 and QSFP_LED_CR0 are tied together

Rev 1 PCBs LED nets QSFP_LED_CG1 and QSFP_LED_CR1 are tied together

3.2 Clocking

The ADM-PCIE-9H7 provides flexible reference clock solutions for the many multi-gigabit transceiver quads and FPGA fabric. Any clock out of the Si5338 Clock Synthesizer is re-configurable from either the front panel USB USB Interface or the Alpha Data sysmon FPGA serial port. This allows the user to configure almost any arbitrary clock frequencies during application run time. Maximum clock frequency is 312.5MHz. After a clock is programmed to a certain frequency, that frequency will become the default on power-up.

There are also three available Si5328 jitter attenuators. These can provide clean clocks to all FireFly and QSFP28 quad locations at many clock frequencies. These devices do only use volatile memory, so the FPGA design will need to re-configure the circuits after any power cycle event.

All clock names in the section below can be found in Complete Pinout Table.

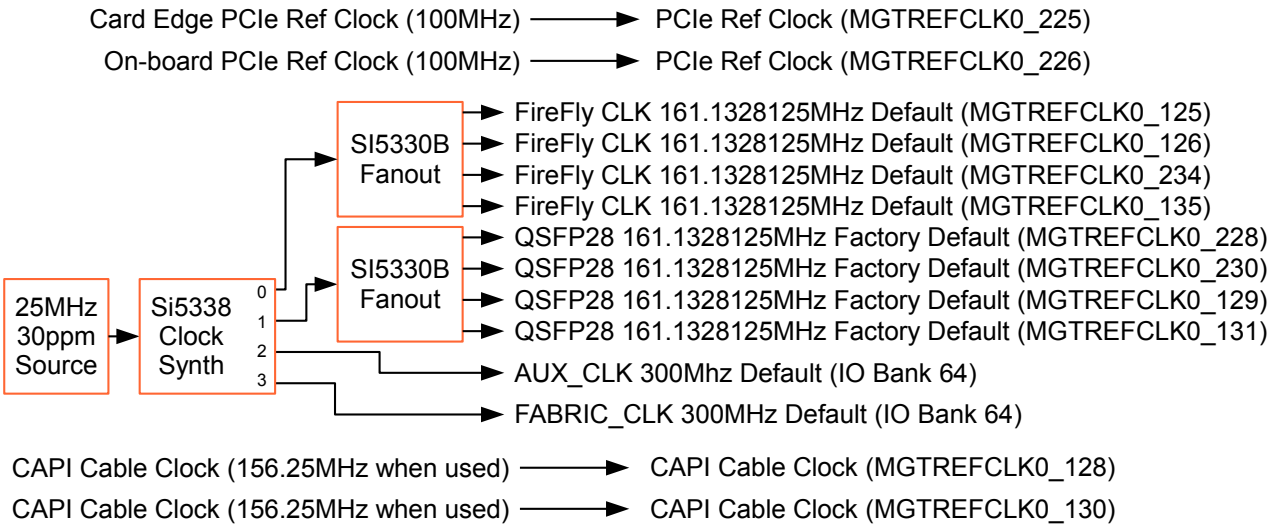

Figure 7 : Clock Topology

3.2.1 Si5328

If jitter attenuation is required please see the reference documentation for the Si5328. https://www.silabs.com/Support%20Documents/TechnicalDocs/Si5328.pdf

See diagram below for net names and configuration settings.

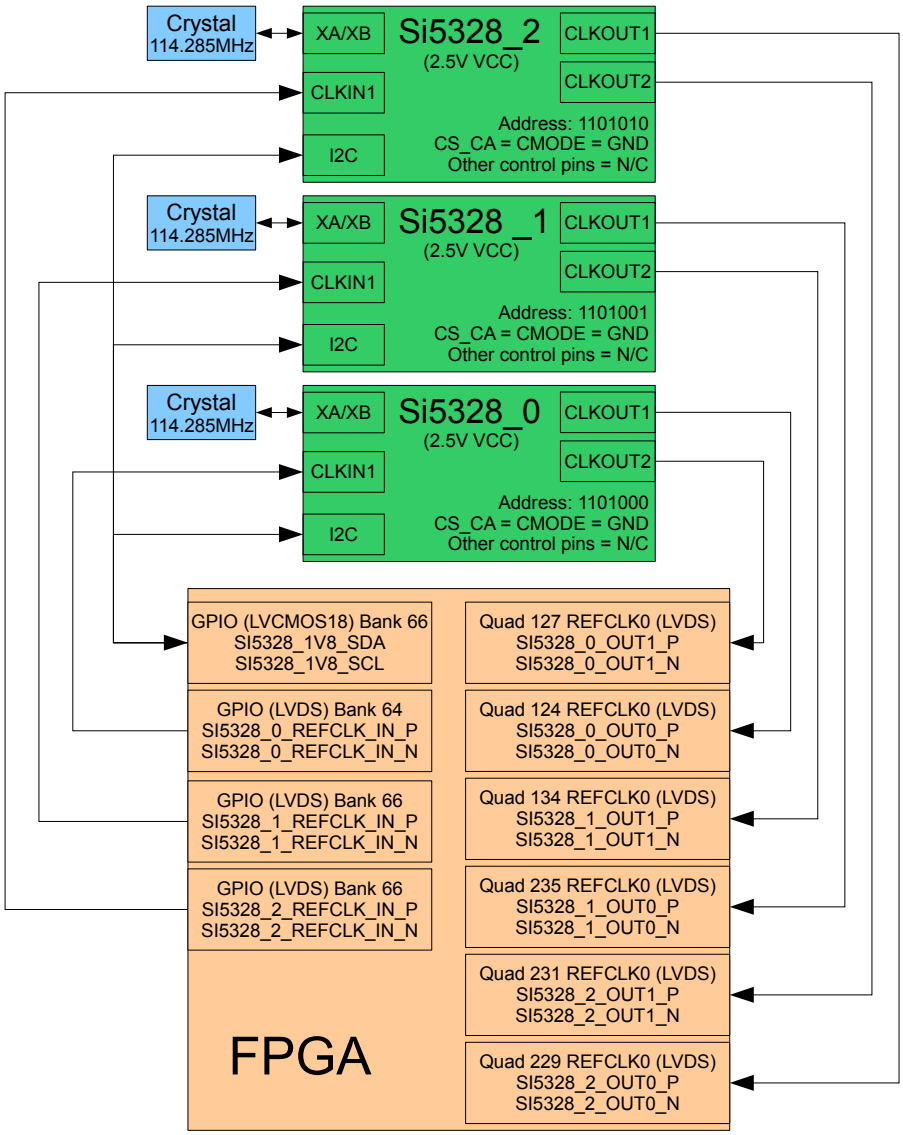

Figure 8 : Si5328 Block Diagram

3.2.2 PCIe Reference Clocks

The 16 MGT lanes connected to the PCIe card edge use MGT tiles 224 through 227 and use the system 100 MHz clock (net name PCIE_REFCLK).

Alternatively, a clean, onboard 100MHz clock is available as well (net name PCIE_LCL_REFCLK).

3.2.3 Fabric Clock

The design offers a fabric clock (net name FABRIC_SRC_CLK) which defaults to 300 MHz. This clock is intended to be used for IDELAY elements in FPGA designs. The fabric clock is connected to a Global Clock (GC) pin.

DIFF_TERM_ADV = TERM_100 is required for LVDS termination

3.2.4 Auxiliary Clock

The design offers a auxiliary clock (net name AUX_CLK) which defaults to 300 MHz. This clock can be used for any purpose and is connected to a Global Clock (GC) pin.

DIFF_TERM_ADV = TERM_100 is required for LVDS termination

3.2.5 Programming Clock (EMCCLK)

A 100MHz clock (net name EMCCLK_B) is fed into the EMCCLK pin to drive the SPI flash device during configuration of the FPGA. Note that this is not a global clock capable IO pin.

3.2.6 QSFP28

The QSFP28 cages are located in MGT tiles 228 through 231 and use a 161.1328125MHz default reference clock. Note that this clock frequency can be changed to any arbitrary clock frequency up to 312MHz by re-programing the Si5338 reprogrammable clock oscillator via system monitor. This can be done using the Alpha Data API or over USB with the appropriate Alpha Data Software tools.

See net names QSFP_CLK_0 and QSFP_CLK_1 for pin locations.

The QSFP28 cages are also located such that they can be clocked from a Si5328 jitter attenuator clock multiplier.

See net names SI5328_2_OUT0 and SI5328_2_OUT1 for pin locations.

3.2.7 Ultraport SlimSAS (OpenCAPI)

The Ultraport SlimSAS connectors are located in MGT tile 128 through 131.

For OpenCAPI an external 156.25MHz clock is provided over the cable.

See net names CAPI_0_CLK1 and CAPI_1_CLK1 for pin locations.

For other applications, this clock is shared with the QSFP clock from the Si5328 clock synthesizer (defaults to 161.1328125MHz).

See net names QSFP_CLK_2 and QSFP_CLK_3 for pin locations.

3.2.8 FireFly

Eight FireFly connectors use MGT quads 124-127, 134-135, and 234-235 (134-135 and 234-235 are not present in VU35P).

All eight quads can access the shared FireFly reference clock, which is independent from all other onboard clocks, and defaults to 161.1328125MHz.

See net names FIREFLY_CLK_0, FIREFLY_CLK_1, FIREFLY_CLK_2, FIREFLY_CLK_3 for pin locations.

Alternatively, two of the Si5328 clock synthesizers are connected to the FireFly quads.

See net names SI5328_0_OUT0, SI5328_0_OUT1, SI5328_1_OUT0, and SI5328_1_OUT1 for pin locations.

3.3 PCI Express

The ADM-PCIE-9H7 is capable of PCIe Gen 1/2/3 with 1/2/4/8/16 lanes. The FPGA drives these lanes directly using the Integrated PCI Express block from Xilinx. Negotiation of PCIe link speed and number of lanes used is generally automatic and does not require user intervention.

PCI Express reset (PERST#) connected to the FPGA at one location. See Complete Pinout Table signals PERST0_1V8_L.

The other pin assignments for the high speed lanes are provided in the pinout attached to the Complete Pinout Table

The PCI Express specification requires that all add-in cards be ready for enumeration within 120ms after power is valid (100ms after power is valid + 20ms after PERST is released). The ADM-PCIE-9H7 does meet this requirement when configured from a tandem bitstream with the proper SPI constraints detailed in the section: Configuration From Flash Memory. For more details on tandem configuration, see Xilinx xapp 1179.

Note:
Different motherboards/backplanes will benefit from different RX equalization schemes within the PCIe IP core provided by Xilinx. Alpha Data recommends using the following setting if a user experiences link errors or training issues with their system: within the IP core generator, change the mode to "Advanced" and open the "GT Settings" tab, change the "form factor driven insertion loss adjustment" from "Add-in Card" to "Chip-to-Chip" (See Xilinx PG239 for more details).

3.4 QSFP28

4 QSFP28 cages are available at the front panel. All cages are capable of housing either active optical or passive copper QSFP28 or QSFP compatible components. The communication interface can run at up to 28Gbps per channel. There are 16 channels between the 4 QSFP28 cages (total maximum bandwidth of 448Gbps). These cages are ideally suited for 16x 10G/25G, 4x 100G Ethernet, or any other protocol supported by the Xilinx GTY Transceivers. Please see Xilinx User Guide UG578 for more details on the capabilities of the transceivers.

All QSFP28 cages have control signals connected to the FPGA. Their connectivity is detailed in the Complete Pinout Table at the end of this document. The notation used to differentiate between cages in the pin assignments is QSFP_A_*, QSFP_B_*, QSFP_C*, and QSFP_D* with locations clarified in the diagram below.

To communicate with the QSFP module register space, use the QSFP_*_SDA_1V8 and QSFP_*_SCL_1V8 as detailed in Complete Pinout Table.

Note:
The LP_MODE (Low Power Mode) to each QSFP28 cage is tied to ground.

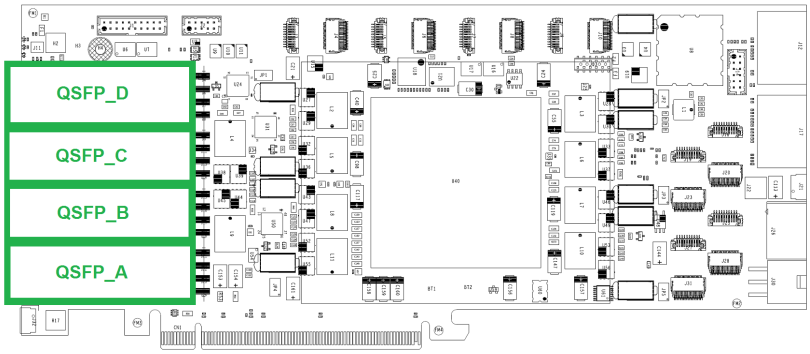

Figure 9 : QSFP Locations

It is possible for Alpha Data to pre-fit the ADM-PCIE-9H7 with QSFP28 optical transceivers. The table below shows the part number for the transceivers fitted when ordered with this board.

Order Code	Description	Part Number	Manufacturer
Q10	40G (4x10) QSFP Optical Transceiver	FTL410QE2C	Finisar
Q14	56G (4x14) QSFP Optical Transceiver	FTL414QB2C	Finisar
Q25	100G (4x25) QSFP28 Optical Transceiver	FTLC9551REPM	Finisar

Table 6 : QSFP28 Part Numbers

3.5 FireFly

8 FireFly sites are available on the circuit board. All sites are capable of hosting either active optical or passive copper FireFly connectors. The communication interface can run at up to 28Gbps per channel in either medium. There are 32 channels between the 8 FireFly sites (total maximum bandwidth of 896Gbps). These cages are ideally suited for 32x 10G/25G, 8x 100G Ethernet, or any other protocol supported by the Xilinx GTY Transceivers. Please see Xilinx User Guide UG578 for more details on the capabilities of the transceivers.

All FireFly sites have control signals connected to the FPGA. Their connectivity is detailed in the Complete Pinout Table at the end of this document. The notation used in the pin assignments is FIREFLY* with locations clarified in the diagram below.

To communicate with the optical module register space, use the FIREFLY*_SDA_1V8 and FIREFLY*_SCL_1V8 as detailed in Complete Pinout Table.

To install new FireFly modules, the top shroud will need to be temporarily or permanently removed. See Top Shroud Removal for details.

Note:
If the ADM-PCIE-9H7 is fitted with a VU35P FPGA (non-standard) then FireFly interfaced 4-7 are not connected.

Figure 10 : FireFly Locations

3.5.1 QSFP Expansion

Alpha Data part number AD-PCIE-FQSFP is available to expand the QSFP slot availability on the ADM-PCIE-9H7 from 4 to up to 12. These cards utilize the samtec FQSFP product https://www.samtec.com/products/fqsfp

Each QSFP slot can house a passive or optical QSFP cable, and are controllable over I2C using the GPIO expansion capabilities of the ADM-PCIE-9H7.

These slots are suitable for 100Gbps Ethernet or any other similar high speed protocol.

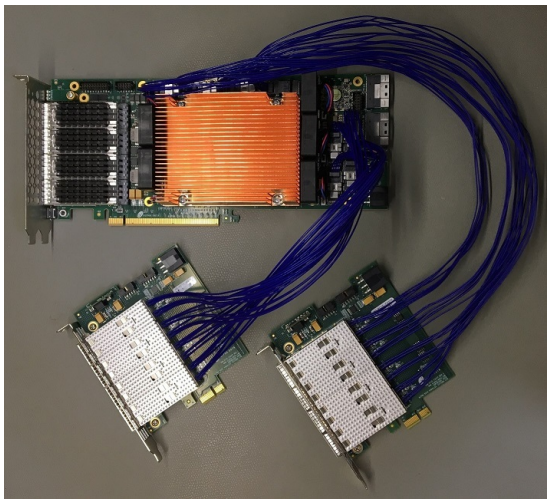

Figure 11 : FQSFP connections

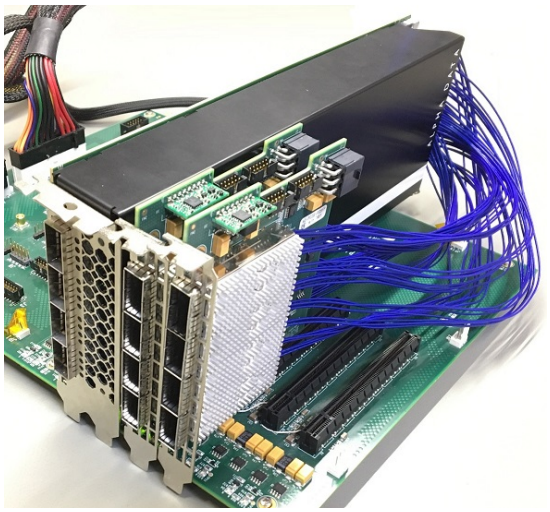

Figure 12 : FQSFP with shroud

3.6 OpenCAPI Ultraport SlimSAS

An Ultraport SlimSAS receptacles along the back of the board allow for OpenCAPI compliant interfaces running at 200G (8 chanels at 25G). Please contact support@alpha-data.com or your IBM representative for more details on OpenCAPI and its benefits.

The SlimSAS connector can also be used to connect multiple 9H7 cards within a chassis.

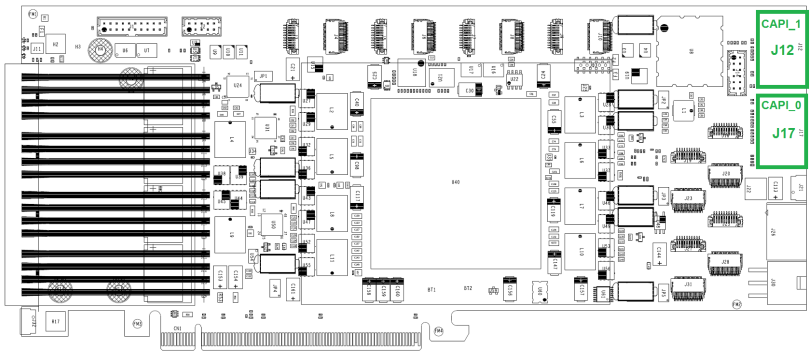

Figure 13 : OpenCAPI Location

3.7 System Monitor

The ADM-PCIE-9H7 has the ability to monitor temperature, voltage, and current of the system to check on the operation of the board. The monitoring is implemented using an Atmel AVR microcontroller.

If the core FPGA temperature exceeds 105 degrees Celsius, the FPGA will be cleared to prevent damage to the card.

Control algorithms within the microcontroller automatically check line voltages and on board temperatures and shares makes the information available to the FPGA over a dedicated serial interface built into the Alpha Data reference design package (sold separately). The information can also be accessed directly from the microcontroller over the USB interface on the front panel or via the IPMI interface available at the PCIe card edge.

Monitors	Index	Purpose/Description
ETC	ETC	Elapsed time counter (seconds)
EC	EC	Event counter (power cycles)
12.0V	ADC00	Board Input Supply (Edge Connector)
12.0V	ADC01	Board Input Supply (Auxiliary 6-pin)
12.0V	ADC02	Board Input Supply (Auxiliary 8-pin)
3.3V	ADC03	Board Input Supply (Edge Connector)
3.3V_I	ADC04	3.3V input current in amps
3.3V	ADC05	Board Input Auxiliary Power Supply
2.5V	ADC06	Clock and DRAM Voltage Supply
1.8V	ADC07	FPGA IO Voltage (VCCO)
1.8V	ADC08	Transceiver Power (AVCC_AUX)
1.2V	ADC09	HBM Power
1.2V	ADC10	Transceiver Power (AVTT)
0.9V	ADC11	Transceiver Power (AVCC)
0.85-0.90V	ADC12	BRAM + INT_IO (VccINT_IO)
0.72-0.90V	ADC13	FPGA Core Supply (VccINT)
uC_Temp	TMP00	FPGA on-die temperature
Board0_Temp	TMP01	Board temperature near front panel
Board1_Temp	TMP02	Board temperature near back top corner
FPGA_Temp	TMP03	FPGA on-die temperature

Table 7 : Voltage, Current, and Temperature Monitors

3.7.1 System Monitor Status LEDs

LEDs D2 (Red) and D1 (Green) indicate the card health status.

LEDs	*Status*
Green	Running and no alarms
Green + Red	Standby (Powered off)
Flashing Green + Flashing Red (together)	Attention - critical alarm active
Flashing Green + Flashing Red (alternating)	Service Mode
Flashing Green + Red	Attention - alarm active
Red	Missing application firmware or invalid firmware
Flashing Red	FPGA configuration cleared to protect board

Table 8 : Status LED Definitions

3.7.2 Fan Controllers

The onboard USB bus controlled by the system monitor has access to a MAX6620 fan controller. This device can be controlled through the multiple onboard system monitor communication interfaces, including USB, PCIe Edge SMBUS, and FPGA sysmon seral communication port. The fan controller is on I2C bus 1 at address 0x2a. For additional questions. Contact support@alpha-data.com with additional questions on utilizing these controllers.

3.8 USB Interface

The FPGA can be configured directly from the USB connection on either the front panel or the rear card edge. The ADM-PCIE-9H7 utilizes the Digilent USB-JTAG converter box which is supported by the Xilinx software tool suite. Simply connect a micro-USB AB type cable between the ADM-PCIE-9H7 USB port and a host computer with Vivado installed. Vivado Hardware Manager will automatically recognize the FPGA and allow you to configure the FPGA and the SBPI configuration PROM.

The same USB connector is used to directly access the system monitor system. All voltages, currents, temperatures, and non-volatile clock configuration settings can be accessed using Alpha Data's avr2util software at this interface.

Avr2util for Windows and the associated USB driver is downloadable here: https://support.alpha-data.com/pub/firmware/utilities/windows/

Avr2util for Linux is downloadable here:https://support.alpha-data.com/pub/firmware/utilities/linux/

Use "avr2util.exe /?" to see all options.

For example "avr2util.exe /usbcom \\.\com4 display-sensors" will display all sensor values.

For example "avr2util.exe /usbcom \\.\com4 setclknv 0 156250000" will set the FireFly clock to 156.25MHz. setclk index 0 = FireFly_CLK, setclk index 1 = QSFP_CLK, index 2 = AUX_CLK, index 3 = Fabric_CLK.

Change 'com4' to match the com port number assigned under windows device manager.

3.9 Configuration

There are two main ways of configuring the FPGA on the ADM-PCIE-9H7:

- From Flash memory, at power-on, as described in Section 3.9.1
- Using USB cable connected at either USB port Section 3.9.2

3.9.1 Configuration From Flash Memory

The FPGA can be automatically configured at power-on from two 1 Gbit QSPI flash memory device configured as an x8 SPI device (Micron part numbers MT25QU01GBBB8E12-0SIT). These flash devices are typically divided into two regions of 128 MiByte each, where each region is sufficiently large to hold an uncompressed bitstream for a VU37P FPGA.

The ADM-PCIE-9H7 is shipped with a simple PCIe endpoint bitstream containing a basic Alpha Data ADXDMA bitstream. Alpha Data can load in other custom bitstreams during production test, please contact sales@alpha-data.com for more details.

It is possible to use Multiboot with a fallback image on this hardware. The master SPI configuration interface and the Fallback MultiBoot are discussed in detail in Xilinx UG570.

The flash address map is as detailed below:

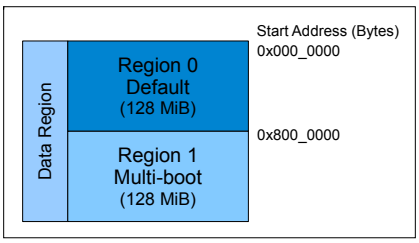

Figure 14 : Flash Address Map

At power-on, the FPGA attempts to configure itself automatically in serial master mode based on the contents of the header in the programing file. Multibook and ICAP can be used to selected between the two configuration regions to be loaded into the FPGA. See Xilinx UG570 MultiBoot for details.

The image loaded can also support tandem PROM or tandem PCIE with field update configuration methods. These options reduce power-on load times to help meet the PCIe reset timing requirements. Tandem with field also enables a host system to reconfigure the user FPGA logic without losing the PCIe link, a useful feature when system resets and power cycles are not an option.

The Alpha Data System Monitor is also capable of reconfiguring the flash memory and reprograming the FPGA. This provides a useful failsafe mechanism to re-program the FPGA even if it drops off the PCIe bus. The system monitor can be accessed over USB at the front panel and rear edge, or over the SMBUS connections on the PCIe edge.

3.9.1.1 Building and Programming Configuration Images

Generate a bitfile with these constraints (see xapp1233):

- set_property BITSTREAM.GENERAL.COMPRESS TRUE [current_design]
- set_property BITSTREAM.CONFIG.EXTMASTERCCLK_EN {DIV-2} [current_design]
- set_property BITSTREAM.CONFIG.SPI_32BIT_ADDR YES [current_design]
- set_property BITSTREAM.CONFIG.SPI_BUSWIDTH 8 [current_design]
- set_property BITSTREAM.CONFIG.SPI_FALL_EDGE YES [current_design]
- set_property BITSTREAM.CONFIG.UNUSEDPIN {Pullnone} [current_design]
- set_property CFGBVS GND [current_design]
- set_property CONFIG_VOLTAGE 1.8 [current_design]
- set_property BITSTREAM.CONFIG.OVERTEMPSHUTDOWN Enable [current_design]

Generate an MCS file with these properties (write_cfgmem):

- -format MCS
- -size 64
- -interface SPIx8
- -loadbit "up 0x0000000 <directory/to/file/filename.bit>" (0th location)
- -loadbit "up 0x8000000 <directory/to/file/filename.bit>" (1st location, optional)

Program with vivado hardware manager with these settings (see xapp1233):

- SPI part: mt25qu01-spi-x1_x2_x4_x8
- State of non-config mem I/O pins: Pull-none
- Target the four files generated from the write_cfgmem tcl command.

3.9.2 Configuration via JTAG

A micro-USB AB Cable may be attached to the front panel or rear edge USB port. This permits the FPGA to be reconfigured using the Xilinx Vivado Hardware Manager via the integrated Digilent JTAG converter box. The device will be automatically recognized in Vivado Hardware Manager.

For more detailed instructions, please see “Using a Vivado Hardware Manager to Program an FPGA Device” section of Xilinx UG908: https://www.xilinx.com/support/documentation/sw_manuals/xilinx2014_1/ug908-vivado-programming-debugging.pdf

3.10 GPIO Connector

The GPIO option consists of a versatile shrouded connector from Molex with part number 87832-2020 that give users with custom IO requirements four direct connect to FPGA signals.

Recommended mating plug: Molex 87568-2093

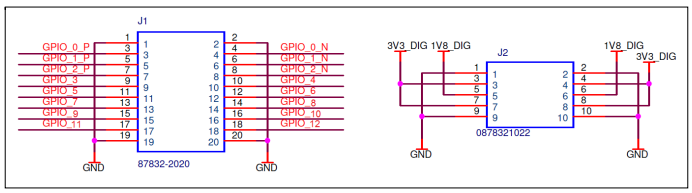

Figure 15 : GPIO Connector Schematic

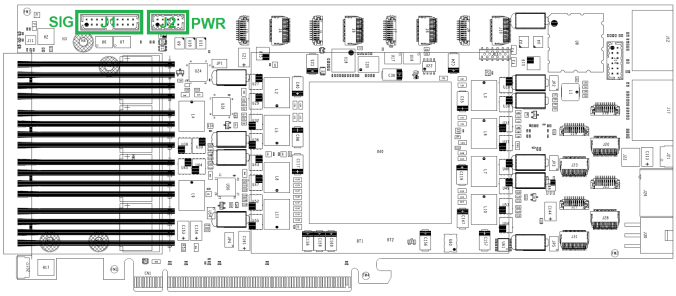

Figure 16 : GPIO Connector Location

3.10.1 Direct Connect FPGA Signals

16 nets are broken out to the GPIO header, 6 as three differential pairs. These signal are suitable for any 1.8V supported signaling standards supported by the Xilinx UltraScale architecture. See Xilinx UG571 for IO options. LVDS and 1.8 CMOS are popular options.

The direct connect GPIO signals are limited to 1.8V by a quickswitch (74CBTLVD3245PW) in order to protect the FPGA from overvoltage on IO pins. This quickswitch allows the signals to travel in either direction with only 4 ohms of series impedance and less than 1ns of propagation delay. The nets are directly connected to the FPGA after the quickswitch.

Direct connect signal names are labeled GP0_1V8_P/N and GP1_1V8_P/N, etc. to show polarity and grouping. The signal pin allocations can be found in Complete Pinout Table

3.10.2 Timing Input

J22 (SMB jack) can be used as an isolated timing input signal (up to 10MHz). Applications can either directly connect to the GPIO connector, or Alpha Data can provide a cabled solution with an SMA or similar connector on the front panel. Contact sales@alpha-data.com for front panel connector options.

For pin locations, see signal name PPS_BUF_1V8 in Complete Pinout Table.

The signal is isolated through a optical isolator part number ACPL-M61L with a 739 ohm of series resistance.

3.11 User EEPROM

A 2Kb I2C user EEPROM is provided for storing MAC addresses or other user information. The EEPROM is part number CAT34C02HU4IGT4A

The address pins A2, A1, and A0 are all strapped to a logical '0'.

Write protect (WP), Serial Clock (SCL), and Serial Data (SDA) pin assignments can be found in Complete Pinout Table with the names SPARE_WP, SPARE_SCL, and SPARE_SDA respectively.

WP, SDA, and SCL signals all have external pull-up resistors on the card.

3.12 Battery Backed Encryption

Two coin cell batter holders are available to provide voltage to the VBATT pin of the FPGA. When at least one battery is populated, the FPGA can hold an AES encryption key to guarantee the security of user IP. See Xilinx UG570, chapter 8 for more details.

Two battery holders are present to allow hot swapping and battery replacement without losing the key information within the FPGA.

Use a battery cell of less than 2.0V (NOT lithium chemistry) with 6.8mm diameter and between 2.1 and 2.6mm in height (i.e. SR621 or SR626 type).

The battery slots are not filled by default. Please contact sales@alpha-data.com to have these fitted prior to shipping.

The batteries can be accessed by removing the top shroud, see Top Shroud Removal for details.

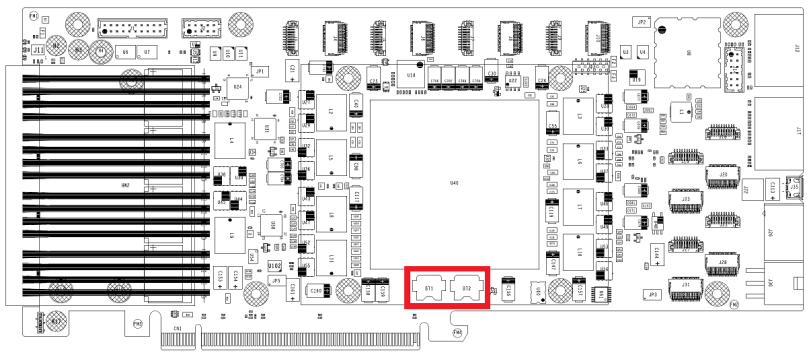

Figure 17 : Top Shroud Screws

3.12.1 Top Shroud Removal

The board can be accessed by removing the top shroud using a 1/16" hex driver. Remove the 7 button head screws shown in the image below. Do not remove the other screws. The shroud will then lift straight up with no resistance for passive cooling configurations. Active cooling configurations will have fan connections that will resist removal after about 30mm. These four plugs can be safely removed to allow for complete board access. When re-installing, plug the fans back in with the shroud assembly hovering about 30mm above the top of the circuit board before installing the screws.

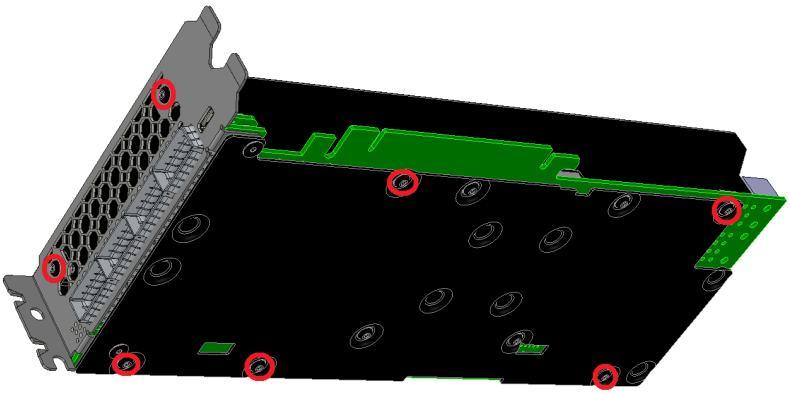

Figure 18 : Top Shroud Screws

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Appendix A: Complete Pinout Table

Pin Number	Signal Name	Pin Name	Bank Voltage
BK9	AUX_CLK_PIN_N	IO_L12N_T1U_N11_GC_68	1.8 (LVDS with DIFF_TERM_ADV)
BJ9	AUX_CLK_PIN_P	IO_L12P_T1U_N10_GC_68	1.8 (LVDS with DIFF_TERM_ADV)
BN50	AVR_B2U_1V8	IO_L2P_T0L_N2_66	1.8 (LVCMOS18)
BP48	AVR_HS_B2U_1V8	IO_L1P_T0L_N0_DBC_66	1.8 (LVCMOS18)
BH50	AVR_HS_CLK_1V8	IO_L12N_T1U_N11_GC_66	1.8 (LVCMOS18)
BP49	AVR_HS_U2B_1V8	IO_L1N_T0L_N1_DBC_66	1.8 (LVCMOS18)
BH49	AVR_MON_CLK_1V8	IO_L12P_T1U_N10_GC_66	1.8 (LVCMOS18)
BN51	AVR_U2B_1V8	IO_L2N_T0L_N3_66	1.8 (LVCMOS18)
AJ41	CAPI_0_CLK1_PIN_N	MGTREFCLK0N_128	MGT REFCLK
AJ40	CAPI_0_CLK1_PIN_P	MGTREFCLK0P_128	MGT REFCLK
BM29	CAPI_0_I2C_SCL_1V8	IO_L1N_T0L_N1_DBC_64	1.8 (LVCMOS18)
BM28	CAPI_0_I2C_SDA_1V8	IO_L1P_T0L_N0_DBC_64	1.8 (LVCMOS18)
BN31	CAPI_0_INT/RESET_1V8	IO_L3P_T0L_N4_AD15P_64	1.8 (LVCMOS18)
AL50	CAPI_0_RX0_N	MGTYRXN0_128	MGT
AL49	CAPI_0_RX0_P	MGTYRXP0_128	MGT
AK52	CAPI_0_RX1_N	MGTYRXN1_128	MGT
AK51	CAPI_0_RX1_P	MGTYRXP1_128	MGT
AE50	CAPI_0_RX10_N	MGTYRXN3_129	MGT
AE49	CAPI_0_RX10_P	MGTYRXP3_129	MGT
AJ54	CAPI_0_RX2_N	MGTYRXN2_128	MGT
AJ53	CAPI_0_RX2_P	MGTYRXP2_128	MGT
AH52	CAPI_0_RX3_N	MGTYRXN3_128	MGT
AH51	CAPI_0_RX3_P	MGTYRXP3_128	MGT
AG54	CAPI_0_RX7_N	MGTYRXN0_129	MGT
AG53	CAPI_0_RX7_P	MGTYRXP0_129	MGT
AF52	CAPI_0_RX8_N	MGTYRXN1_129	MGT
AF51	CAPI_0_RX8_P	MGTYRXP1_129	MGT
AE54	CAPI_0_RX9_N	MGTYRXN2_129	MGT
AE53	CAPI_0_RX9_P	MGTYRXP2_129	MGT
AK47	CAPI_0_TX0_N	MGTYTXN0_128	MGT
AK46	CAPI_0_TX0_P	MGTYTXP0_128	MGT
AJ49	CAPI_0_TX1_N	MGTYTXN1_128	MGT

Table 9 : Complete Pinout Table (continued on next page)

Pin Number	Signal Name	Pin Name	Bank Voltage
AJ48	CAPI_0_TX1_P	MGTYTXP1_128	MGT
AE45	CAPI_0_TX10_N	MGTYTXN3_129	MGT
AE44	CAPI_0_TX10_P	MGTYTXP3_129	MGT
AJ45	CAPI_0_TX2_N	MGTYTXN2_128	MGT
AJ44	CAPI_0_TX2_P	MGTYTXP2_128	MGT
AH47	CAPI_0_TX3_N	MGTYTXN3_128	MGT
AH46	CAPI_0_TX3_P	MGTYTXP3_128	MGT
AG49	CAPI_0_TX7_N	MGTYTXN0_129	MGT
AG48	CAPI_0_TX7_P	MGTYTXP0_129	MGT
AG45	CAPI_0_TX8_N	MGTYTXN1_129	MGT
AG44	CAPI_0_TX8_P	MGTYTXP1_129	MGT
AF47	CAPI_0_TX9_N	MGTYTXN2_129	MGT
AF46	CAPI_0_TX9_P	MGTYTXP2_129	MGT
AD43	CAPI_1_CLK1_PIN_N	MGTREFCLK0N_130	MGT REFCLK
AD42	CAPI_1_CLK1_PIN_P	MGTREFCLK0P_130	MGT REFCLK
BP29	CAPI_1_I2C_SCL_1V8	IO_L2N_T0L_N3_64	1.8 (LVCMOS18)
BP28	CAPI_1_I2C_SDA_1V8	IO_L2P_T0L_N2_64	1.8 (LVCMOS18)
BP31	CAPI_1_INT/RESET_1V8	IO_L3N_T0L_N5_AD15N_64	1.8 (LVCMOS18)
AD52	CAPI_1_RX0_N	MGTYRXN0_130	MGT
AD51	CAPI_1_RX0_P	MGTYRXP0_130	MGT
AC54	CAPI_1_RX1_N	MGTYRXN1_130	MGT
AC53	CAPI_1_RX1_P	MGTYRXP1_130	MGT
V52	CAPI_1_RX10_N	MGTYRXN3_131	MGT
V51	CAPI_1_RX10_P	MGTYRXP3_131	MGT
AC50	CAPI_1_RX2_N	MGTYRXN2_130	MGT
AC49	CAPI_1_RX2_P	MGTYRXP2_130	MGT
AB52	CAPI_1_RX3_N	MGTYRXN3_130	MGT
AB51	CAPI_1_RX3_P	MGTYRXP3_130	MGT
AA54	CAPI_1_RX7_N	MGTYRXN0_131	MGT
AA53	CAPI_1_RX7_P	MGTYRXP0_131	MGT
Y52	CAPI_1_RX8_N	MGTYRXN1_131	MGT
Y51	CAPI_1_RX8_P	MGTYRXP1_131	MGT
W54	CAPI_1_RX9_N	MGTYRXN2_131	MGT
W53	CAPI_1_RX9_P	MGTYRXP2_131	MGT
AD47	CAPI_1_TX0_N	MGTYTXN0_130	MGT
AD46	CAPI_1_TX0_P	MGTYTXP0_130	MGT

Table 9 : Complete Pinout Table (continued on next page)

Pin Number	Signal Name	Pin Name	Bank Voltage
AC45	CAPI_1_TX1_N	MGTYTXN1_130	MGT
AC44	CAPI_1_TX1_P	MGTYTXP1_130	MGT
W45	CAPI_1_TX10_N	MGTYTXN3_131	MGT
W44	CAPI_1_TX10_P	MGTYTXP3_131	MGT
AB47	CAPI_1_TX2_N	MGTYTXN2_130	MGT
AB46	CAPI_1_TX2_P	MGTYTXP2_130	MGT
AA49	CAPI_1_TX3_N	MGTYTXN3_130	MGT
AA48	CAPI_1_TX3_P	MGTYTXP3_130	MGT
AA45	CAPI_1_TX7_N	MGTYTXN0_131	MGT
AA44	CAPI_1_TX7_P	MGTYTXP0_131	MGT
Y47	CAPI_1_TX8_N	MGTYTXN1_131	MGT
Y46	CAPI_1_TX8_P	MGTYTXP1_131	MGT
W49	CAPI_1_TX9_N	MGTYTXN2_131	MGT
W48	CAPI_1_TX9_P	MGTYTXP2_131	MGT
BD14	CCLK	CCLK_0	STARTUPE3
BE43	EMCCLK_B	IO_L24P_T3U_N10_EMCCLK_65	1.8 (LVCMOS18)
BJ53	FABRIC_SRC_CLK_PIN_N	IO_L13N_T2L_N1_GC_QBC_66	1.8 (LVDS with DIFF_TERM_ADV)
BJ52	FABRIC_SRC_CLK_PIN_P	IO_L13P_T2L_N0_GC_QBC_66	1.8 (LVDS with DIFF_TERM_ADV)
AR41	FIREFLY_CLK_0_PIN_N	MGTREFCLK0N_125	MGT REFCLK
AR40	FIREFLY_CLK_0_PIN_P	MGTREFCLK0P_125	MGT REFCLK
AN41	FIREFLY_CLK_1_PIN_N	MGTREFCLK0N_126	MGT REFCLK
AN40	FIREFLY_CLK_1_PIN_P	MGTREFCLK0P_126	MGT REFCLK
T12**	FIREFLY_CLK_2_PIN_N	MGTREFCLK0N_234	MGT REFCLK
T13**	FIREFLY_CLK_2_PIN_P	MGTREFCLK0P_234	MGT REFCLK
P43**	FIREFLY_CLK_3_PIN_N	MGTREFCLK0N_135	MGT REFCLK
P42**	FIREFLY_CLK_3_PIN_P	MGTREFCLK0P_135	MGT REFCLK
BG10	FIREFLY0_MODPRS_L	IO_L21P_T3L_N4_AD8P_68	1.8 (LVCMOS18)
AY52	FIREFLY0_RX0_N	MGTYRXN0_125	MGT
AY51	FIREFLY0_RX0_P	MGTYRXP0_125	MGT
AW54	FIREFLY0_RX1_N	MGTYRXN1_125	MGT
AW53	FIREFLY0_RX1_P	MGTYRXP1_125	MGT
AW50	FIREFLY0_RX2_N	MGTYRXN2_125	MGT
AW49	FIREFLY0_RX2_P	MGTYRXP2_125	MGT
AV52	FIREFLY0_RX3_N	MGTYRXN3_125	MGT

Table 9 : Complete Pinout Table (continued on next page)

Pin Number	Signal Name	Pin Name	Bank Voltage
AV51	FIREFLY0_RX3_P	MGTYRXP3_125	MGT
BP11	FIREFLY0_SCL_1V8	IO_L1N_T0L_N1_DBC_68	1.8 (LVCMOS18)
BP12	FIREFLY0_SDA_1V8	IO_L1P_T0L_N0_DBC_68	1.8 (LVCMOS18)
AY47	FIREFLY0_TX0_N	MGTYTXN0_125	MGT
AY46	FIREFLY0_TX0_P	MGTYTXP0_125	MGT
AW45	FIREFLY0_TX1_N	MGTYTXN1_125	MGT
AW44	FIREFLY0_TX1_P	MGTYTXP1_125	MGT
AV47	FIREFLY0_TX2_N	MGTYTXN2_125	MGT
AV46	FIREFLY0_TX2_P	MGTYTXP2_125	MGT
AU45	FIREFLY0_TX3_N	MGTYTXN3_125	MGT
AU44	FIREFLY0_TX3_P	MGTYTXP3_125	MGT
BG9	FIREFLY1_MODPRS_L	IO_L21N_T3L_N5_AD8N_68	1.8 (LVCMOS18)
BC54	FIREFLY1_RX0_N	MGTYRXN0_124	MGT
BC53	FIREFLY1_RX0_P	MGTYRXP0_124	MGT
BB52	FIREFLY1_RX1_N	MGTYRXN1_124	MGT
BB51	FIREFLY1_RX1_P	MGTYRXP1_124	MGT
BA54	FIREFLY1_RX2_N	MGTYRXN2_124	MGT
BA53	FIREFLY1_RX2_P	MGTYRXP2_124	MGT
BA50	FIREFLY1_RX3_N	MGTYRXN3_124	MGT
BA49	FIREFLY1_RX3_P	MGTYRXP3_124	MGT
BP13	FIREFLY1_SCL_1V8	IO_L2N_T0L_N3_68	1.8 (LVCMOS18)
BP14	FIREFLY1_SDA_1V8	IO_L2P_T0L_N2_68	1.8 (LVCMOS18)
BC49	FIREFLY1_TX0_N	MGTYTXN0_124	MGT
BC48	FIREFLY1_TX0_P	MGTYTXP0_124	MGT
BC45	FIREFLY1_TX1_N	MGTYTXN1_124	MGT
BC44	FIREFLY1_TX1_P	MGTYTXP1_124	MGT
BB47	FIREFLY1_TX2_N	MGTYTXN2_124	MGT
BB46	FIREFLY1_TX2_P	MGTYTXP2_124	MGT
BA45	FIREFLY1_TX3_N	MGTYTXN3_124	MGT
BA44	FIREFLY1_TX3_P	MGTYTXP3_124	MGT
BF12	FIREFLY2_MODPRS_L	IO_L22P_T3U_N6_DBC_AD0P_68	1.8 (LVCMOS18)
AU54	FIREFLY2_RX0_N	MGTYRXN0_126	MGT
AU53	FIREFLY2_RX0_P	MGTYRXP0_126	MGT
AT52	FIREFLY2_RX1_N	MGTYRXN1_126	MGT
AT51	FIREFLY2_RX1_P	MGTYRXP1_126	MGT
AR54	FIREFLY2_RX2_N	MGTYRXN2_126	MGT

Table 9 : Complete Pinout Table (continued on next page)

Pin Number	Signal Name	Pin Name	Bank Voltage
AR53	FIREFLY2_RX2_P	MGTYRXP2_126	MGT
AP52	FIREFLY2_RX3_N	MGTYRXN3_126	MGT
AP51	FIREFLY2_RX3_P	MGTYRXP3_126	MGT
BN12	FIREFLY2_SCL_1V8	IO_L3N_T0L_N5_AD15N_68	1.8 (LVCMOS18)
BM12	FIREFLY2_SDA_1V8	IO_L3P_T0L_N4_AD15P_68	1.8 (LVCMOS18)
AU49	FIREFLY2_TX0_N	MGTYTXN0_126	MGT
AU48	FIREFLY2_TX0_P	MGTYTXP0_126	MGT
AT47	FIREFLY2_TX1_N	MGTYTXN1_126	MGT
AT46	FIREFLY2_TX1_P	MGTYTXP1_126	MGT
AR49	FIREFLY2_TX2_N	MGTYTXN2_126	MGT
AR48	FIREFLY2_TX2_P	MGTYTXP2_126	MGT
AR45	FIREFLY2_TX3_N	MGTYTXN3_126	MGT
AR44	FIREFLY2_TX3_P	MGTYTXP3_126	MGT
BF11	FIREFLY3_MODPRS_L	IO_L22N_T3U_N7_DBC_AD0N_68	1.8 (LVCMOS18)
AN54	FIREFLY3_RX0_N	MGTYRXN0_127	MGT
AN53	FIREFLY3_RX0_P	MGTYRXP0_127	MGT
AN50	FIREFLY3_RX1_N	MGTYRXN1_127	MGT
AN49	FIREFLY3_RX1_P	MGTYRXP1_127	MGT
AM52	FIREFLY3_RX2_N	MGTYRXN2_127	MGT
AM51	FIREFLY3_RX2_P	MGTYRXP2_127	MGT
AL54	FIREFLY3_RX3_N	MGTYRXN3_127	MGT
AL53	FIREFLY3_RX3_P	MGTYRXP3_127	MGT
BN14	FIREFLY3_SCL_1V8	IO_L4N_T0U_N7_DBC_AD7N_68	1.8 (LVCMOS18)
BN15	FIREFLY3_SDA_1V8	IO_L4P_T0U_N6_DBC_AD7P_68	1.8 (LVCMOS18)
AP47	FIREFLY3_TX0_N	MGTYTXN0_127	MGT
AP46	FIREFLY3_TX0_P	MGTYTXP0_127	MGT
AN45	FIREFLY3_TX1_N	MGTYTXN1_127	MGT
AN44	FIREFLY3_TX1_P	MGTYTXP1_127	MGT
AM47	FIREFLY3_TX2_N	MGTYTXN2_127	MGT
AM46	FIREFLY3_TX2_P	MGTYTXP2_127	MGT
AL45	FIREFLY3_TX3_N	MGTYTXN3_127	MGT
AL44	FIREFLY3_TX3_P	MGTYTXP3_127	MGT
BE11	FIREFLY4_MODPRS_L	IO_L23P_T3U_N8_68	1.8 (LVCMOS18)
L1**	FIREFLY4_RX0_N	MGTYRXN0_234	MGT
L2**	FIREFLY4_RX0_P	MGTYRXP0_234	MGT
K3**	FIREFLY4_RX1_N	MGTYRXN1_234	MGT

Table 9 : Complete Pinout Table (continued on next page)

Pin Number	Signal Name	Pin Name	Bank Voltage
K4**	FIREFLY4_RX1_P	MGTYRXP1_234	MGT
J1**	FIREFLY4_RX2_N	MGTYRXN2_234	MGT
J2**	FIREFLY4_RX2_P	MGTYRXP2_234	MGT
H3**	FIREFLY4_RX3_N	MGTYRXN3_234	MGT
H4**	FIREFLY4_RX3_P	MGTYRXP3_234	MGT
BM13	FIREFLY4_SCL_1V8	IO_L5N_T0U_N9_AD14N_68	1.8 (LVCMOS18)
BM14	FIREFLY4_SDA_1V8	IO_L5P_T0U_N8_AD14P_68	1.8 (LVCMOS18)
L6**	FIREFLY4_TX0_N	MGTYTXN0_234	MGT
L7**	FIREFLY4_TX0_P	MGTYTXP0_234	MGT
L10**	FIREFLY4_TX1_N	MGTYTXN1_234	MGT
L11**	FIREFLY4_TX1_P	MGTYTXP1_234	MGT
K8**	FIREFLY4_TX2_N	MGTYTXN2_234	MGT
K9**	FIREFLY4_TX2_P	MGTYTXP2_234	MGT
J6**	FIREFLY4_TX3_N	MGTYTXN3_234	MGT
J7**	FIREFLY4_TX3_P	MGTYTXP3_234	MGT
BF10	FIREFLY5_MODPRS_L	IO_L23N_T3U_N9_68	1.8 (LVCMOS18)
G1**	FIREFLY5_RX0_N	MGTYRXN0_235	MGT
G2**	FIREFLY5_RX0_P	MGTYRXP0_235	MGT
F3**	FIREFLY5_RX1_N	MGTYRXN1_235	MGT
F4**	FIREFLY5_RX1_P	MGTYRXP1_235	MGT
E1**	FIREFLY5_RX2_N	MGTYRXN2_235	MGT
E2**	FIREFLY5_RX2_P	MGTYRXP2_235	MGT
D3**	FIREFLY5_RX3_N	MGTYRXN3_235	MGT
D4**	FIREFLY5_RX3_P	MGTYRXP3_235	MGT
BM15	FIREFLY5_SCL_1V8	IO_L6N_T0U_N11_AD6N_68	1.8 (LVCMOS18)
BL15	FIREFLY5_SDA_1V8	IO_L6P_T0U_N10_AD6P_68	1.8 (LVCMOS18)
G6**	FIREFLY5_TX0_N	MGTYTXN0_235	MGT
G7**	FIREFLY5_TX0_P	MGTYTXP0_235	MGT
E6**	FIREFLY5_TX1_N	MGTYTXN1_235	MGT
E7**	FIREFLY5_TX1_P	MGTYTXP1_235	MGT
C6**	FIREFLY5_TX2_N	MGTYTXN2_235	MGT
C7**	FIREFLY5_TX2_P	MGTYTXP2_235	MGT
A5**	FIREFLY5_TX3_N	MGTYTXN3_235	MGT
A6**	FIREFLY5_TX3_P	MGTYTXP3_235	MGT
BE10	FIREFLY6_MODPRS_L	IO_L24P_T3U_N10_68	1.8 (LVCMOS18)
G54**	FIREFLY6_RX0_N	MGTYRXN0_135	MGT

Table 9 : Complete Pinout Table (continued on next page)

Pin Number	Signal Name	Pin Name	Bank Voltage
G53**	FIREFLY6_RX0_P	MGTYRXP0_135	MGT
F52**	FIREFLY6_RX1_N	MGTYRXN1_135	MGT
F51**	FIREFLY6_RX1_P	MGTYRXP1_135	MGT
E54**	FIREFLY6_RX2_N	MGTYRXN2_135	MGT
E53**	FIREFLY6_RX2_P	MGTYRXP2_135	MGT
D52**	FIREFLY6_RX3_N	MGTYRXN3_135	MGT
D51**	FIREFLY6_RX3_P	MGTYRXP3_135	MGT
BP9	FIREFLY6_SCL_1V8	IO_L7P_T1L_N0_QBC_AD13P_68	1.8 (LVCMOS18)
BN11	FIREFLY6_SDA_1V8	IO_T0U_N12_VRP_68	1.8 (LVCMOS18)
G49**	FIREFLY6_TX0_N	MGTYTXN0_135	MGT
G48**	FIREFLY6_TX0_P	MGTYTXP0_135	MGT
E49**	FIREFLY6_TX1_N	MGTYTXN1_135	MGT
E48**	FIREFLY6_TX1_P	MGTYTXP1_135	MGT
C49**	FIREFLY6_TX2_N	MGTYTXN2_135	MGT
C48**	FIREFLY6_TX2_P	MGTYTXP2_135	MGT
A50**	FIREFLY6_TX3_N	MGTYTXN3_135	MGT
A49**	FIREFLY6_TX3_P	MGTYTXP3_135	MGT
BE9	FIREFLY7_MODPRS_L	IO_L24N_T3U_N11_68	1.8 (LVCMOS18)
L54**	FIREFLY7_RX0_N	MGTYRXN0_134	MGT
L53**	FIREFLY7_RX0_P	MGTYRXP0_134	MGT
K52**	FIREFLY7_RX1_N	MGTYRXN1_134	MGT
K51**	FIREFLY7_RX1_P	MGTYRXP1_134	MGT
J54**	FIREFLY7_RX2_N	MGTYRXN2_134	MGT
J53**	FIREFLY7_RX2_P	MGTYRXP2_134	MGT
H52**	FIREFLY7_RX3_N	MGTYRXN3_134	MGT
H51**	FIREFLY7_RX3_P	MGTYRXP3_134	MGT
BM10	FIREFLY7_SCL_1V8	IO_L8P_T1L_N2_AD5P_68	1.8 (LVCMOS18)
BP8	FIREFLY7_SDA_1V8	IO_L7N_T1L_N1_QBC_AD13N_68	1.8 (LVCMOS18)
L49**	FIREFLY7_TX0_N	MGTYTXN0_134	MGT
L48**	FIREFLY7_TX0_P	MGTYTXP0_134	MGT
L45**	FIREFLY7_TX1_N	MGTYTXN1_134	MGT
L44**	FIREFLY7_TX1_P	MGTYTXP1_134	MGT
K47**	FIREFLY7_TX2_N	MGTYTXN2_134	MGT
K46**	FIREFLY7_TX2_P	MGTYTXP2_134	MGT
J49**	FIREFLY7_TX3_N	MGTYTXN3_134	MGT
J48**	FIREFLY7_TX3_P	MGTYTXP3_134	MGT

Table 9 : Complete Pinout Table (continued on next page)

Pin Number	Signal Name	Pin Name	Bank Voltage
BC15	FPGA_FLASH_CE0_L	RDWR_FCS_B_0	STARTUPE3
BP47	FPGA_FLASH_CE1_L	IO_L2N_T0L_N3_FWE_FCS2_B_65	1.8 (LVCMOS18)
AW15	FPGA_FLASH_DQ0	D00_MOSI_0	STARTUPE3
AY15	FPGA_FLASH_DQ1	D01_DIN_0	STARTUPE3
AY14	FPGA_FLASH_DQ2	D02_0	STARTUPE3
AY13	FPGA_FLASH_DQ3	D03_0	STARTUPE3
BE45	FPGA_FLASH_DQ4	IO_L22P_T3U_N6_DBC_AD0P-_D04_65	1.8 (LVCMOS18)
BE46	FPGA_FLASH_DQ5	IO_L22N_T3U_N7_DBC_AD0N-_D05_65	1.8 (LVCMOS18)
BF42	FPGA_FLASH_DQ6	IO_L21P_T3L_N4_AD8P_D06_65	1.8 (LVCMOS18)
BF43	FPGA_FLASH_DQ7	IO_L21N_T3L_N5_AD8N_D07_65	1.8 (LVCMOS18)
BJ32	GPIO_0_1V8_N	IO_L13N_T2L_N1_GC_QBC_64	1.8 (LVDS or LVCMOS18)
BH32	GPIO_0_1V8_P	IO_L13P_T2L_N0_GC_QBC_64	1.8 (LVDS or LVCMOS18)
BF36	GPIO_1_1V8_N	IO_L17N_T2U_N9_AD10N_64	1.8 (LVDS or LVCMOS18)
BF35	GPIO_1_1V8_P	IO_L17P_T2U_N8_AD10P_64	1.8 (LVDS or LVCMOS18)
BG32	GPIO_10	IO_L21N_T3L_N5_AD8N_64	1.8 (LVCMOS18)
BF32	GPIO_11	IO_L23P_T3U_N8_64	1.8 (LVCMOS18)
BK30	GPIO_12	IO_L22N_T3U_N7_DBC_AD0N_64	1.8 (LVCMOS18)
BH35	GPIO_2_1V8_N	IO_L18N_T2U_N11_AD2N_64	1.8 (LVDS or LVCMOS18)
BH34	GPIO_2_1V8_P	IO_L18P_T2U_N10_AD2P_64	1.8 (LVDS or LVCMOS18)
BG29	GPIO_3	IO_L19P_T3L_N0_DBC_AD9P_64	1.8 (LVCMOS18)
BG33	GPIO_4	IO_T2U_N12_64	1.8 (LVCMOS18)
BH29	GPIO_5	IO_L20P_T3L_N2_AD1P_64	1.8 (LVCMOS18)
BG30	GPIO_6	IO_L19N_T3L_N1_DBC_AD9N_64	1.8 (LVCMOS18)
BF31	GPIO_7	IO_L21P_T3L_N4_AD8P_64	1.8 (LVCMOS18)
BH30	GPIO_8	IO_L20N_T3L_N3_AD1N_64	1.8 (LVCMOS18)
BJ29	GPIO_9	IO_L22P_T3U_N6_DBC_AD0P_64	1.8 (LVCMOS18)
BJ31	OPTICAL_INT_1V8_L	IO_L24N_T3U_N11_64	1.8 (LVCMOS18)
BK29	OPTICAL_RST_1V8_L	IO_T3U_N12_64	1.8 (LVCMOS18)
AN14	PCIE_LCL_REFCLK_PIN_N	MGTREFCLK0N_226	MGT REFCLK
AN15	PCIE_LCL_REFCLK_PIN_P	MGTREFCLK0P_226	MGT REFCLK
AR14	PCIE_REFCLK_PIN_N	MGTREFCLK0N_225	MGT REFCLK
AR15	PCIE_REFCLK_PIN_P	MGTREFCLK0P_225	MGT REFCLK
AL1	PCIE_RX0_N	MGTYRXN3_227	MGT
AL2	PCIE_RX0_P	MGTYRXP3_227	MGT

Table 9 : Complete Pinout Table (continued on next page)

Pin Number	Signal Name	Pin Name	Bank Voltage
AM3	PCIE_RX1_N	MGTYRXN2_227	MGT
AM4	PCIE_RX1_P	MGTYRXP2_227	MGT
AW1	PCIE_RX10_N	MGTYRXN1_225	MGT
AW2	PCIE_RX10_P	MGTYRXP1_225	MGT
AY3	PCIE_RX11_N	MGTYRXN0_225	MGT
AY4	PCIE_RX11_P	MGTYRXP0_225	MGT
BA5	PCIE_RX12_N	MGTYRXN3_224	MGT
BA6	PCIE_RX12_P	MGTYRXP3_224	MGT
BA1	PCIE_RX13_N	MGTYRXN2_224	MGT
BA2	PCIE_RX13_P	MGTYRXP2_224	MGT
BB3	PCIE_RX14_N	MGTYRXN1_224	MGT
BB4	PCIE_RX14_P	MGTYRXP1_224	MGT
BC1	PCIE_RX15_N	MGTYRXN0_224	MGT
BC2	PCIE_RX15_P	MGTYRXP0_224	MGT
AN5	PCIE_RX2_N	MGTYRXN1_227	MGT
AN6	PCIE_RX2_P	MGTYRXP1_227	MGT
AN1	PCIE_RX3_N	MGTYRXN0_227	MGT
AN2	PCIE_RX3_P	MGTYRXP0_227	MGT
AP3	PCIE_RX4_N	MGTYRXN3_226	MGT
AP4	PCIE_RX4_P	MGTYRXP3_226	MGT
AR1	PCIE_RX5_N	MGTYRXN2_226	MGT
AR2	PCIE_RX5_P	MGTYRXP2_226	MGT
AT3	PCIE_RX6_N	MGTYRXN1_226	MGT
AT4	PCIE_RX6_P	MGTYRXP1_226	MGT
AU1	PCIE_RX7_N	MGTYRXN0_226	MGT
AU2	PCIE_RX7_P	MGTYRXP0_226	MGT
AV3	PCIE_RX8_N	MGTYRXN3_225	MGT
AV4	PCIE_RX8_P	MGTYRXP3_225	MGT
AW5	PCIE_RX9_N	MGTYRXN2_225	MGT
AW6	PCIE_RX9_P	MGTYRXP2_225	MGT
AL10	PCIE_TX0_PIN_N	MGTYTXN3_227	MGT
AL11	PCIE_TX0_PIN_P	MGTYTXP3_227	MGT
AM8	PCIE_TX1_PIN_N	MGTYTXN2_227	MGT
AM9	PCIE_TX1_PIN_P	MGTYTXP2_227	MGT
AW10	PCIE_TX10_PIN_N	MGTYTXN1_225	MGT
AW11	PCIE_TX10_PIN_P	MGTYTXP1_225	MGT

Table 9 : Complete Pinout Table (continued on next page)

Pin Number	Signal Name	Pin Name	Bank Voltage
AY8	PCIE_TX11_PIN_N	MGTYTXN0_225	MGT
AY9	PCIE_TX11_PIN_P	MGTYTXP0_225	MGT
BA10	PCIE_TX12_PIN_N	MGTYTXN3_224	MGT
BA11	PCIE_TX12_PIN_P	MGTYTXP3_224	MGT
BB8	PCIE_TX13_PIN_N	MGTYTXN2_224	MGT
BB9	PCIE_TX13_PIN_P	MGTYTXP2_224	MGT
BC10	PCIE_TX14_PIN_N	MGTYTXN1_224	MGT
BC11	PCIE_TX14_PIN_P	MGTYTXP1_224	MGT
BC6	PCIE_TX15_PIN_N	MGTYTXN0_224	MGT
BC7	PCIE_TX15_PIN_P	MGTYTXP0_224	MGT
AN10	PCIE_TX2_PIN_N	MGTYTXN1_227	MGT
AN11	PCIE_TX2_PIN_P	MGTYTXP1_227	MGT
AP8	PCIE_TX3_PIN_N	MGTYTXN0_227	MGT
AP9	PCIE_TX3_PIN_P	MGTYTXP0_227	MGT
AR10	PCIE_TX4_PIN_N	MGTYTXN3_226	MGT
AR11	PCIE_TX4_PIN_P	MGTYTXP3_226	MGT
AR6	PCIE_TX5_PIN_N	MGTYTXN2_226	MGT
AR7	PCIE_TX5_PIN_P	MGTYTXP2_226	MGT
AT8	PCIE_TX6_PIN_N	MGTYTXN1_226	MGT
AT9	PCIE_TX6_PIN_P	MGTYTXP1_226	MGT
AU10	PCIE_TX7_PIN_N	MGTYTXN0_226	MGT
AU11	PCIE_TX7_PIN_P	MGTYTXP0_226	MGT
AU6	PCIE_TX8_PIN_N	MGTYTXN3_225	MGT
AU7	PCIE_TX8_PIN_P	MGTYTXP3_225	MGT
AV8	PCIE_TX9_PIN_N	MGTYTXN2_225	MGT
AV9	PCIE_TX9_PIN_P	MGTYTXP2_225	MGT
BF41	PERST0_1V8_L	IO_T3U_N12_PERSTN0_65	1.8 (LVCMOS18)
BG50	PPS_BUF_1V8	IO_L20N_T3L_N3_AD1N_66	1.8 (LVCMOS18)
BJ54	PWR_SENSE_PIN	IO_L16N_T2U_N7_QBC_AD3N_66	1.8 (LVCMOS18)
BH54	PWR_SENSE0_PIN	IO_L16P_T2U_N6_QBC_AD3P_66	1.8 (LVCMOS18)
BK54	PWR_SENSE1_PIN	IO_L15N_T2L_N5_AD11N_66	1.8 (LVCMOS18)
BN35	QSFP_A_MODPRS_L	IO_L7N_T1L_N1_QBC_AD13N_64	1.8 (LVCMOS18)
AL5	QSFP_A_RX0_N	MGTYRXN0_228	MGT
AL6	QSFP_A_RX0_P	MGTYRXP0_228	MGT
AK3	QSFP_A_RX1_N	MGTYRXN1_228	MGT
AK4	QSFP_A_RX1_P	MGTYRXP1_228	MGT

Table 9 : Complete Pinout Table (continued on next page)

Pin Number	Signal Name	Pin Name	Bank Voltage
AJ1	QSFP_A_RX2_N	MGTYRXN2_228	MGT
AJ2	QSFP_A_RX2_P	MGTYRXP2_228	MGT
AH3	QSFP_A_RX3_N	MGTYRXN3_228	MGT
AH4	QSFP_A_RX3_P	MGTYRXP3_228	MGT
BN29	QSFP_A_SCL_1V8	IO_L4P_T0U_N6_DBC_AD7P_64	1.8 (LVCMOS18)
BN30	QSFP_A_SDA_1V8	IO_L4N_T0U_N7_DBC_AD7N_64	1.8 (LVCMOS18)
AK8	QSFP_A_TX0_N	MGTYTXN0_228	MGT
AK9	QSFP_A_TX0_P	MGTYTXP0_228	MGT
AJ6	QSFP_A_TX1_N	MGTYTXN1_228	MGT
AJ7	QSFP_A_TX1_P	MGTYTXP1_228	MGT
AJ10	QSFP_A_TX2_N	MGTYTXN2_228	MGT
AJ11	QSFP_A_TX2_P	MGTYTXP2_228	MGT
AH8	QSFP_A_TX3_N	MGTYTXN3_228	MGT
AH9	QSFP_A_TX3_P	MGTYTXP3_228	MGT
BN34	QSFP_B_MODPRS_L	IO_L8P_T1L_N2_AD5P_64	1.8 (LVCMOS18)
AG1	QSFP_B_RX0_N	MGTYRXN0_229	MGT
AG2	QSFP_B_RX0_P	MGTYRXP0_229	MGT
AF3	QSFP_B_RX1_N	MGTYRXN1_229	MGT
AF4	QSFP_B_RX1_P	MGTYRXP1_229	MGT
AE1	QSFP_B_RX2_N	MGTYRXN2_229	MGT
AE2	QSFP_B_RX2_P	MGTYRXP2_229	MGT
AE5	QSFP_B_RX3_N	MGTYRXN3_229	MGT
AE6	QSFP_B_RX3_P	MGTYRXP3_229	MGT
BL30	QSFP_B_SCL_1V8	IO_L5P_T0U_N8_AD14P_64	1.8 (LVCMOS18)
BM30	QSFP_B_SDA_1V8	IO_L5N_T0U_N9_AD14N_64	1.8 (LVCMOS18)
AG6	QSFP_B_TX0_N	MGTYTXN0_229	MGT
AG7	QSFP_B_TX0_P	MGTYTXP0_229	MGT
AG10	QSFP_B_TX1_N	MGTYTXN1_229	MGT
AG11	QSFP_B_TX1_P	MGTYTXP1_229	MGT
AF8	QSFP_B_TX2_N	MGTYTXN2_229	MGT
AF9	QSFP_B_TX2_P	MGTYTXP2_229	MGT
AE10	QSFP_B_TX3_N	MGTYTXN3_229	MGT
AE11	QSFP_B_TX3_P	MGTYTXP3_229	MGT
BP34	QSFP_C_MODPRS_L	IO_L8N_T1L_N3_AD5N_64	1.8 (LVCMOS18)
AD3	QSFP_C_RX0_N	MGTYRXN0_230	MGT
AD4	QSFP_C_RX0_P	MGTYRXP0_230	MGT

Table 9 : Complete Pinout Table (continued on next page)

Pin Number	Signal Name	Pin Name	Bank Voltage
AC1	QSFP_C_RX1_N	MGTYRXN1_230	MGT
AC2	QSFP_C_RX1_P	MGTYRXP1_230	MGT
AC5	QSFP_C_RX2_N	MGTYRXN2_230	MGT
AC6	QSFP_C_RX2_P	MGTYRXP2_230	MGT
AB3	QSFP_C_RX3_N	MGTYRXN3_230	MGT
AB4	QSFP_C_RX3_P	MGTYRXP3_230	MGT
BN32	QSFP_C_SCL_1V8	IO_L6P_T0U_N10_AD6P_64	1.8 (LVCMOS18)
BP32	QSFP_C_SDA_1V8	IO_L6N_T0U_N11_AD6N_64	1.8 (LVCMOS18)
AD8	QSFP_C_TX0_N	MGTYTXN0_230	MGT
AD9	QSFP_C_TX0_P	MGTYTXP0_230	MGT
AC10	QSFP_C_TX1_N	MGTYTXN1_230	MGT
AC11	QSFP_C_TX1_P	MGTYTXP1_230	MGT
AB8	QSFP_C_TX2_N	MGTYTXN2_230	MGT
AB9	QSFP_C_TX2_P	MGTYTXP2_230	MGT
AA6	QSFP_C_TX3_N	MGTYTXN3_230	MGT
AA7	QSFP_C_TX3_P	MGTYTXP3_230	MGT
AJ14	QSFP_CLK_0_PIN_N	MGTREFCLK0N_228	MGT REFCLK
AJ15	QSFP_CLK_0_PIN_P	MGTREFCLK0P_228	MGT REFCLK
AD12	QSFP_CLK_1_PIN_N	MGTREFCLK0N_230	MGT REFCLK
AD13	QSFP_CLK_1_PIN_P	MGTREFCLK0P_230	MGT REFCLK
AG41	QSFP_CLK_2_PIN_N	MGTREFCLK0N_129	MGT REFCLK
AG40	QSFP_CLK_2_PIN_P	MGTREFCLK0P_129	MGT REFCLK
AB43	QSFP_CLK_3_PIN_N	MGTREFCLK0N_131	MGT REFCLK
AB42	QSFP_CLK_3_PIN_P	MGTREFCLK0P_131	MGT REFCLK
BL32	QSFP_D_MODPRS_L	IO_L9P_T1L_N4_AD12P_64	1.8 (LVCMOS18)
AA1	QSFP_D_RX0_N	MGTYRXN0_231	MGT
AA2	QSFP_D_RX0_P	MGTYRXP0_231	MGT
Y3	QSFP_D_RX1_N	MGTYRXN1_231	MGT
Y4	QSFP_D_RX1_P	MGTYRXP1_231	MGT
W1	QSFP_D_RX2_N	MGTYRXN2_231	MGT
W2	QSFP_D_RX2_P	MGTYRXP2_231	MGT
V3	QSFP_D_RX3_N	MGTYRXN3_231	MGT
V4	QSFP_D_RX3_P	MGTYRXP3_231	MGT
BM32	QSFP_D_SCL_1V8	IO_T0U_N12_VRP_64	1.8 (LVCMOS18)
BM34	QSFP_D_SDA_1V8	IO_L7P_T1L_N0_QBC_AD13P_64	1.8 (LVCMOS18)
AA10	QSFP_D_TX0_N	MGTYTXN0_231	MGT

Table 9 : Complete Pinout Table (continued on next page)

Pin Number	Signal Name	Pin Name	Bank Voltage
AA11	QSFP_D_TX0_P	MGTYTXP0_231	MGT
Y8	QSFP_D_TX1_N	MGTYTXN1_231	MGT
Y9	QSFP_D_TX1_P	MGTYTXP1_231	MGT
W6	QSFP_D_TX2_N	MGTYTXN2_231	MGT
W7	QSFP_D_TX2_P	MGTYTXP2_231	MGT
W10	QSFP_D_TX3_N	MGTYTXN3_231	MGT
W11	QSFP_D_TX3_P	MGTYTXP3_231	MGT
BN49	QSFP_LED_AG0_1V8	IO_L3N_T0L_N5_AD15N_66	1.8 (LVCMOS18)
BM49	QSFP_LED_AG1_1V8	IO_L4P_T0U_N6_DBC_AD7P_66	1.8 (LVCMOS18)
BK48	QSFP_LED_AR0_1V8	IO_L7P_T1L_N0_QBC_AD13P_66	1.8 (LVCMOS18)
BK49	QSFP_LED_AR1_1V8	IO_L7N_T1L_N1_QBC_AD13N_66	1.8 (LVCMOS18)
BM50	QSFP_LED_BG0_1V8	IO_L4N_T0U_N7_DBC_AD7N_66	1.8 (LVCMOS18)
BL51	QSFP_LED_BG1_1V8	IO_L5P_T0U_N8_AD14P_66	1.8 (LVCMOS18)
BK50	QSFP_LED_BR0_1V8	IO_L8P_T1L_N2_AD5P_66	1.8 (LVCMOS18)
BK51	QSFP_LED_BR1_1V8	IO_L8N_T1L_N3_AD5N_66	1.8 (LVCMOS18)
BM52	QSFP_LED_CG0_1V8	IO_L5N_T0U_N9_AD14N_66	1.8 (LVCMOS18)
BJ48	QSFP_LED_CG0_1V8	IO_L9P_T1L_N4_AD12P_66	1.8 (LVCMOS18)
BL52	QSFP_LED_CG1_1V8	IO_L6P_T0U_N10_AD6P_66	1.8 (LVCMOS18)
BJ49	QSFP_LED_CG1_1V8	IO_L9N_T1L_N5_AD12N_66	1.8 (LVCMOS18)
BL53	QSFP_LED_DG0_1V8	IO_L6N_T0U_N11_AD6N_66	1.8 (LVCMOS18)
BL50	QSFP_LED_DG1_1V8	IO_T0U_N12_VRP_66	1.8 (LVCMOS18)
BH47	QSFP_LED_DR0_1V8	IO_L10P_T1U_N6_QBC_AD4P_66	1.8 (LVCMOS18)
BJ47	QSFP_LED_DR1_1V8	IO_L10N_T1U_N7_QBC_AD4N_66	1.8 (LVCMOS18)
AV43	SI5328_0_OUT0_PIN_N	MGTREFCLK0N_124	MGT REFCLK
AV42	SI5328_0_OUT0_PIN_P	MGTREFCLK0P_124	MGT REFCLK
AL41	SI5328_0_OUT1_PIN_N	MGTREFCLK0N_127	MGT REFCLK
AL40	SI5328_0_OUT1_PIN_P	MGTREFCLK0P_127	MGT REFCLK
BL33	SI5328_0_REFCLK_IN_N	IO_L12N_T1U_N11_GC_64	MGT REFCLK
BK33	SI5328_0_REFCLK_IN_P	IO_L12P_T1U_N10_GC_64	MGT REFCLK
P12**	SI5328_1_OUT0_PIN_N	MGTREFCLK0N_235	MGT REFCLK
P13**	SI5328_1_OUT0_PIN_P	MGTREFCLK0P_235	MGT REFCLK
T43**	SI5328_1_OUT1_PIN_N	MGTREFCLK0N_134	MGT REFCLK
T42**	SI5328_1_OUT1_PIN_P	MGTREFCLK0P_134	MGT REFCLK
BJ51	SI5328_1_REFCLK_IN_N	IO_L11N_T1U_N9_GC_66	MGT REFCLK
BH51	SI5328_1_REFCLK_IN_P	IO_L11P_T1U_N8_GC_66	MGT REFCLK
BG54	SI5328_1V8_SCL	IO_L17N_T2U_N9_AD10N_66	MGT REFCLK

Table 9 : Complete Pinout Table (continued on next page)

Pin Number	Signal Name	Pin Name	Bank Voltage
BG53	SI5328_1V8_SDA	IO_L17P_T2U_N8_AD10P_66	MGT REFCLK
AG14	SI5328_2_OUT0_PIN_N	MGTREFCLK0N_229	MGT REFCLK
AG15	SI5328_2_OUT0_PIN_P	MGTREFCLK0P_229	MGT REFCLK
AB12	SI5328_2_OUT1_PIN_N	MGTREFCLK0N_231	MGT REFCLK
AB13	SI5328_2_OUT1_PIN_P	MGTREFCLK0P_231	MGT REFCLK
BH52	SI5328_2_REFCLK_IN_N	IO_L14N_T2L_N3_GC_66	MGT REFCLK
BG52	SI5328_2_REFCLK_IN_P	IO_L14P_T2L_N2_GC_66	MGT REFCLK
BF51	SI5328_RST_1V8_L	IO_L21P_T3L_N4_AD8P_66	1.8 (LVCMOS18)
BE49	SPARE_SCL	IO_L23P_T3U_N8_66	1.8 (LVCMOS18)
BE50	SPARE_SDA	IO_L23N_T3U_N9_66	1.8 (LVCMOS18)
BD51	SPARE_WP	IO_L24P_T3U_N10_66	1.8 (LVCMOS18)
BM48	SRVC_MD_L_1V8	IO_L3P_T0L_N4_AD15P_66	1.8 (LVCMOS18)
BF53	USER_LED_G0_1V8	IO_T2U_N12_66	1.8 (LVCMOS18)
BG48	USER_LED_G1_1V8	IO_L19P_T3L_N0_DBC_AD9P_66	1.8 (LVCMOS18)
BG49	USER_LED_G2_1V8	IO_L19N_T3L_N1_DBC_AD9N_66	1.8 (LVCMOS18)
BE54	USER_LED_G3_1V8	IO_L18N_T2U_N11_AD2N_66	1.8 (LVCMOS18)
BE53	USER_LED_R0_1V8	IO_L18P_T2U_N10_AD2P_66	1.8 (LVCMOS18)
BF52	USR_SW_0	IO_L21N_T3L_N5_AD8N_66	1.8 (LVCMOS18)
BF47	USR_SW_1	IO_L22P_T3U_N6_DBC_AD0P_66	1.8 (LVCMOS18)

Table 9 : Complete Pinout Table

** Pin fields marked are not present in VU35P (FireFly 4-7)

Appendix B: SlimSAS Board to Board Cable

There is a cable that can be used to link multiple ADM-PCIE-9H7 boards toghether through the OpenCAPI connector. See below for the associated cable drawing.

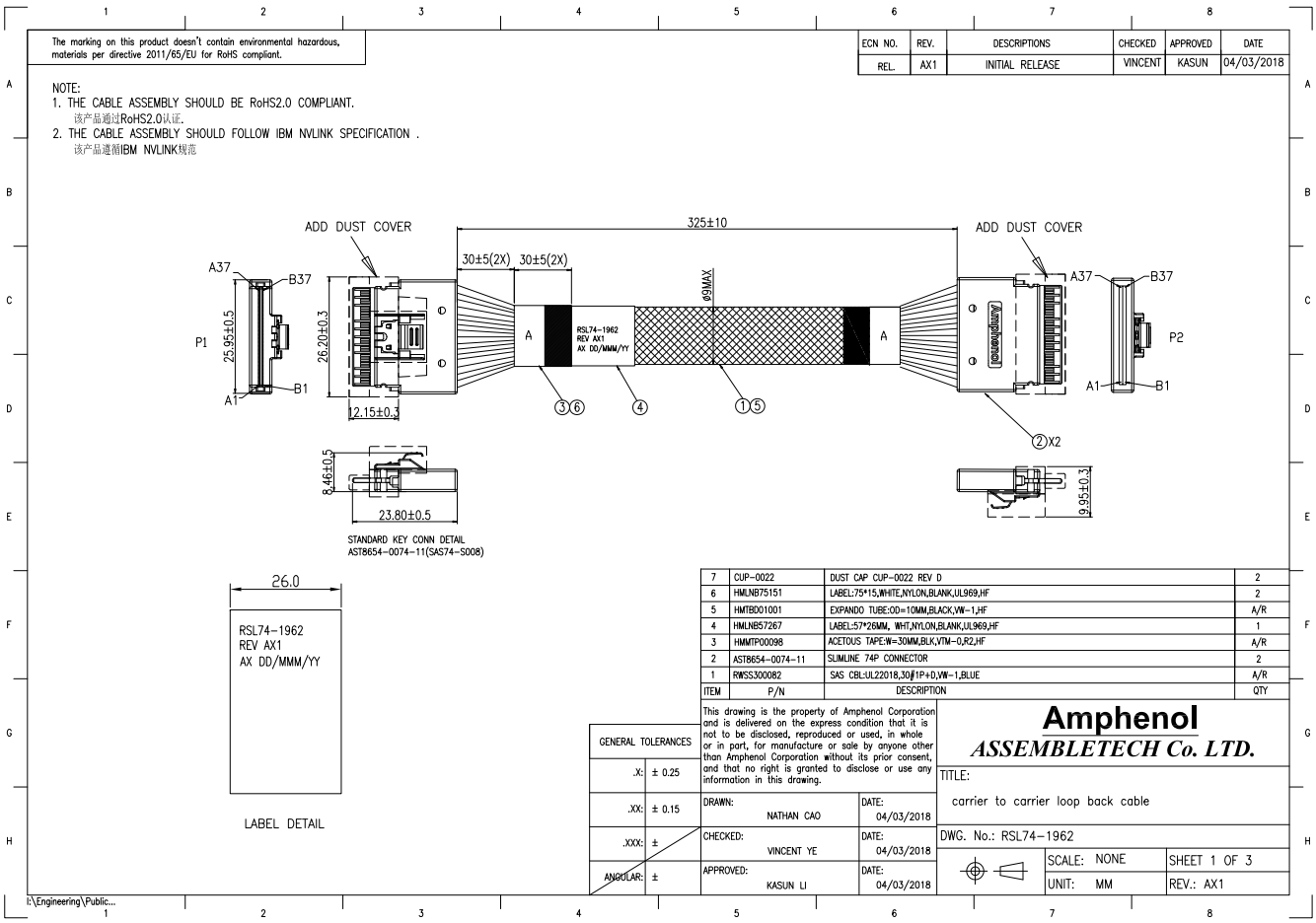

Figure 19 : SlimSAS Board to Board Cable

Revision History

Date	Revision	Changed By	Nature of Change
17 Jul 2018	1.0	K. Roth	Initial Release
20 Sep 2018	1.1	K. Roth	Added thermal data, added FQSFP details, added link to linux avr2util.
19 Oct 2018	1.2	K. Roth	Added section Battery Backed Encryption, corrected grammatical errors, clarified FireFly site reduction from 8 to 4 with VU35P
10 Jun 2019	1.3	K. Roth	Corrected LED labeling mistakes in section LEDs
28 Jul 2022	1.4	K. Roth	Clarified section Power Requirements in that both the PCIE AUX power cable and the PCIE edge are required for the baord to power on.
17 Jul 2023	1.5	K. Roth	Corrected clock index numbers in USB Interface for setclk commands, add table for PCB dimmension in Board Information
19 Mar 2024	1.6	K. Roth	Removed text about an OpenCAPI Ultraport SlimSAS to QSFP expansion board in section OpenCAPI Ultraport SlimSAS.
31 Dec 2024	1.7	K. Roth	Added cable drawing in appendex for SlimSAS Board to Board Cable and included notation in front of com port identifier for avr2util commands.

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